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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,435	03/04/2002	Andrew Carter	1232.010US1	6308

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,435	CARTER ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,7,13,14,17-19 and 21-24* is/are rejected.

7)☒ Claim(s) *4,5,8-12,15,16,20,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 9 is objected to because of the following informalities: claim 9 recites the claimed subject matter "*the decision logic module*", which lacks antecedent basis. Claim 9 should depends on claim 8 instead. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Popplewell et al. US. 6,608,871 B2.

Regarding claim 1, referring to figure 4, in column 4, lines 10-50, Popplewell et al. teaches in figure 4, a data slicer 22 comprising a threshold slicer 60, first and second digital switches 61, 62, and a state logic device 63 and a state to slice converter device 64.

A threshold slicer 10 receives a digital line 10 input. The threshold slicer 10 corresponds to the claimed a sample and hold circuit for receiving and holding

a phase signal that represents a signal from a phase detector as shown in figure 3.

A digital switch 62 is connected to the threshold slicer 60 for pass the phase signal from the threshold slicer 60 in adjusting the timing signal.

The state logic device 63 is connected to digital switch 61. Popplewell et al. does not expressly teach the state logic device 63 detecting good signal transitions, and actuating the switch as set forth in the application claim. Nevertheless, in column 4, lines 50-67, the state logic device 63 receives the starting state, determined by the logic in the threshold slicer 60 and thereafter sequentially through the states with the frequency of the sampling clock. The state logic device provides on its output line 68 a digital value in the range 1 to 8 corresponding to the current state present in the device 63. In column 5, lines 1-7, the switch 62, after the initial state determination, provides on the output line 27 the signal received on the line 70, the output of the data slicer 22 is determined by the state logic device 63 and the sampling clock and is thus not susceptible to slicing errors occurring in the threshold slicer 60. In view of the foregoing disclosure, the state logic device 22 performs equivalent function of the claimed decision logic module. The digital value in the range 1 to 8 represents good signal transitions and switch 62 only provides on the output line 27 the signal received on the line 70, the output of the data slicer 22 is determined by the state logic device 63 and the sampling clock and is thus not susceptible to slicing errors occurring in the threshold slicer 60.

Regarding claim 2, referring to figure 2, in column 4, lines 45-67, the state logic device 63 contains logic which is able to cycle through states 1 to 8, corresponding to levels L2 L3 L4 L3 L2 L1 L0 L1. The level L2 includes zero crossings that may deviate from phase sampling time less than zero crossings for other transitions.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Popplewell et al. US. 6,608,871 B2.

Regarding claim 3, referring to figure 4, the state logic device is adapted to receive slicer output signals via digital switch 61.

As recited in claim 2, the state logic device 63 contains logic which is able to cycle through states 1 to 8, corresponding to levels L2 L3 L4 L3 L2 L1 L0 L1, which represents ideal sampling points.

Popplewell et al. does not teach the slicer output signals provide logic values for at least two bits. Nevertheless, because there are 4 levels representing sampling points, it would have been obvious for one of ordinary skill in the art at the time of the invention that threshold slicer provides logic values for at least two bits.

The state logic device 63 initiates itself using the starting state so received and thereafter cycles sequentially through the states with the frequency of the sampling clock. The state logic device 63 provides on its output line 68 a digital value in the range 1 to 8 corresponding to the current state present in the device 63.

4. Claims 6-7, 13-14, 17-19 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strolle et al. US. 5,550,596.

Regarding claim 6, Strolle et al. invention is directed to a digital signal processing system for receiving and processing high definition television signal, e.g. Quadrature Amplitude Modulation (QAM) format. Referring to figure 1, in column 3, lines 5-35, the receiver includes:

A slicer 24 for receiving a QAM signal transmitted through a transmission channel;

Rotator 16, error detector 26 and a phase detector and voltage controlled oscillator (VCO) network 28. Units 16, 24, 26, and 28 forms a digital phase locked loop for eliminating the dynamically varying carrier offsets. The phase control unit 28 generates output sine and cosine quadrature correction coefficients based on signals S_i and S_o, which are input and output of slicer 24; see column 4, lines 45-67. Output correction coefficients from phase control unit 28 are provided to inputs of rotator 16 to perform a derotating function for producing baseband output signals from rotator 16. In light of the foregoing discussion, the output correction coefficients from phase control unit 28 is part of

the timing signal for use by slicer 24 in determining the amplitude levels for symbols.

Strolle et al. does not expressly teach the claimed limitation "*detect a phase of the received signal using signal transitions within the received signal*". Nevertheless, as recited above, the phase control unit 28 generates output sine and cosine quadrature correction coefficients based on signals S_i and S_o, and the rotator 16 uses the correction coefficients to perform a derotation for producing baseband output signal. In view of that, one of ordinary skill in the art at the time of the invention would have recognized that the phase control unit 28 detects the phase offset of the received signal based on signal transitions from signals S_i and S_o.

As recited above, the phase control unit 28 determines any carrier offsets and generates output sine and cosine quadrature correction coefficients to adjust the timing signal.

Regarding claim 7, in column 2, lines 30-50, Strolle et al. teaches a 32-QAM system, wherein each quadrant of the constellation contains eight symbols at prescribed coordinates with respect to I and Q quadrature axes.

Regarding claim 13, claim 13 is rejected on the same ground as for claim 6 because of similar scope. Furthermore, in column 4, lines 25-67, the error detector 26, coupled to the slicer output and input, produces an output error signal "E" as a function

of the amount of the offset. The output error signal "E", corresponding to the claimed decision feedback output, is provided to a decision directed feedback equalizer 22 passing the phase signal for good signal transition that is used by a phase detector and VCO unit 28 as shown in figure 1.

Regarding claim 14, claim 14 is rejected on the same ground as for claim 7 because of similar scope.

Regarding claim 17, claim 17 is rejected on the same ground as for claim 6 because of similar scope.

Regarding claim 18, claim 18 is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 19, Strolle et al. teaches a 32-QAM system, wherein each quadrant of the constellation contains eight symbols at prescribed coordinates with respect to I and Q quadrature axes. The signal transition is a good signal transition includes determining whether each of N bits has been toggled during transition as appreciated by one of ordinary skill in the art.

Regarding claim 21, claim 21 is rejected on the same ground as for claim 13 because of similar scope.

Regarding claim 22, claim 22 is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 23, claim 23 is rejected on the same ground as for claim 18 because of similar scope.

Regarding claim 24, claim 24 is rejected on the same ground as for claim 19 because of similar scope.

Allowable Subject Matter

5. Claims 4-5, 8-12, 15-16, 20 and 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cloetens et al. U.S. Patent 5,337,335 discloses "Phase Locked Loop With Frequency Deviation Detector And Decoder Circuit Comprising Such A Phase Locked Loop".

Betts et al. U.S. Patent 6,853,695 discloses "System And Method For Deriving Symbol Timing".

Phanse U.S. Patent 6,798,827 B1 discloses "System And Method For Correcting Offsets In An Analog Receiver Front End".

Shieh U.S. Patent 6,904,559 B2 discloses "Error Correction Method In Full Response Read Channels".

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh cong Tran 06/10/2005

Examiner ~~KHANH~~ TRAN